CLAIM AMENDMENTS

1. (currently amended) A method of exchanging data within a direct memory access [[(DMA)]] arrangement including a plurality of IP blocks, the method comprising ~~(A, B, C), characterized in that it includes~~ the steps of: [[-]]

associating with said IP blocks [[(A, B, C)]] respective DMA modules ~~(IDMA A, IDMA B, IDMA C),~~ each ~~of said DMA modules~~ including an input buffer [[(11A, 11B, 11C)]] and an output buffer [[(12A, 12B, 12C)]]; [[-]]

coupling said respective DMA modules [[(IDMA A, IDMA B, IDMA C)]] over a data transfer facility [[(BUS)]] in a chain arrangement where [[in]] each [[said]] DMA module, other than the last in the chain, has ~~at least one of~~ its respective output buffers [[(12A, 12B)]] coupled to the input buffer [[(11B, 11C)]] of another of said DMA modules downstream in the chain and each of said DMA modules, other than the first in the chain, has its respective input buffer [[(11B, 11C)]] coupled to the output buffer [[(12A, 12B)]] of another of said DMA modules upstream in the chain; [[-]]

causing each of said DMA modules [[(IDMA A, IDMA B, IDMA C)]] to interact with the respective IP block [[(A, B, C)]] by writing data from the input buffer [[(11A, 11B, 11C)]] of the [[I]] DMA module into the respective IP block [[(A, B, C)]] and reading data from the respective IP block [[(A, B, C)]] into the output buffer [[(12A, 12B, 12C)]] of the DMA module; and [[-]]

operating said input [[(11A, 11B, 11C)]] and output [[(12A, 12B, 12C)]] buffers in such a way that: [[-]]

said writing of data from the input buffer [[(11A, 11B, 11C)]] of the DMA module into the respective IP block [[(A, B, C)]] is started when [[said]] the respective input buffer [[(11A, 11B, 11C)]] is at least partly filled with data; and [[-]]

when said reading of data from the respective IP block [[(A, B, C)]] into the output buffer of the DMA module is completed, the data in the output buffer of the DMA module are transferred to the input buffer [[(11B, 11C)]] of the DMA module downstream in the chain or, in the case of the last DMA module in the chain, are provided as output data.

2. (currently amended) The method of claim 1, ~~characterized in that it includes~~ further comprising the steps of: [[-]]

associating [[to]] with said output buffers [[(12A, 12B)]] and input buffers [[(11B, 11C)]] coupled in the chain at least one intermediate block [[(16A, 16B)]] to control data transfer between said coupled buffers; [[-]] and

controlling transfer of data between said coupled buffers over said data transfer facility by [[: -]] issuing at least one request of a requesting buffer for a buffer coupled therewith to

indicate at least one transfer condition selected out of the group consisting of:

data existing to be transferred and enough space existing for receiving said data when transferred; [[-]]

issuing at least one corresponding acknowledgment towards said requesting buffer confirming that the said at least one transfer condition is met; and [[-]]

transferring data between said requesting buffer and said coupled buffer, whereby said data transfer facility [[(BUS)]] is left free between said at least one request and said at least one acknowledgement.

3. (currently amended) The method of either of claims 1 or 2, ~~characterized in that it comprises~~ further comprising the steps of: [[-]]

including a CPU in said arrangement; [[and -]]

using said CPU for transferring data to be processed into the input buffer [[(11A)]] of the first DMA module [[(IDMA A)]] in said chain; and [[-]]

using said CPU for collecting said output data from the output buffer [[(12C)]] of the last DMA module [[(IDMA C)]] in said chain.

4. (currently amended) The method of claim 3, ~~characterized in that it includes~~ further comprising the step of configuring said DMA modules [[(IDMA A, IDMA B, IDMA C)]] via said CPU.

5. (currently amended) Architecture of a direct memory access module [[(IDMA)]] for exchanging data between a plurality of IP blocks, ~~characterized in that it includes~~ the architecture comprising: [[-]]

a data transfer facility [[(BUS)]]; [[-]]

a plurality of respective DMA modules [[(IDMA A, IDMA B, IDMA C)]] associated with said IP blocks, the DMA modules being coupled over said data transfer facility [[(BUS)]], each DMA module including: [[-]]

an input buffer [[(11)]] arranged for writing data into a respective IP block [[(A, B, C)]] and exchanging data with said data transfer facility [[(BUS)]], and [[-]]

an output buffer [[(12)]] arranged for reading data from said respective IP block [[(A, B, C)]] and exchanging data with said data transfer [[s]] facility, ~~(BUS); wherein~~ said DMA modules [[are]] being arranged in a chain so that each of said DMA modules, other than the last in the chain, has ~~at least one of~~ its respective output buffer [[(12A, 12B)]] coupled to the

input buffer [[(11B, 11C)]] of another of said DMA modules downstream in the chain and each of said DMA modules, other than the first in the chain, has its input buffer [[(11B, 11C)]] coupled to the output buffer [[(12A, 12B)]] of another of said DMA modules upstream in the chain.

6. (currently amended) The architecture of claim 5 ~~, characterized in that~~ wherein at least one of said input [[(11)]] and output [[(12)]] buffers has a fixed data width with respect to said data transfers facility [[(BUS)]] and a selectively variable data width with respect to said respective IP blocks [[(A, B, C)]].

7. (currently amended) The architecture of ~~either of~~ claim [[s]] 5 or 6, ~~characterized in that it includes~~ further comprising

a slave interface module [[(18)]] configured for reading from outside the architecture data relating to at least one parameter selected from the group consisting of: [[-]]

how many bits are available for reading in said input buffer [[(11)]], [[-]]

how many bits are present in said input buffer [[(11)]], [[-]]

how many bits are available for reading in said output buffer [[(12)]], and [[-]]

how many bits are present in said output buffer [[(12)]].

8. (currently amended) The architecture of ~~any of claims~~ claim 5 ~~to 7, characterized in that it includes~~ further comprising

a reprogrammable finite state machine [[(13)]] arranged for driving operation of said architecture by taking data from said input buffer [[(11)]], downloading data into said respective IP block [[(A, B, C)]], receiving data from said respective IP block [[(A, B, C)]], and storing data in said output buffer [[(12)]].

9. (currently amended) The architecture of ~~any of claims~~ claim 5 ~~to 8, characterized in that to~~ wherein at least one of said input buffers [[(11)]] and output buffers [[(12)]] [[there]] is associated with a respective master block [[(15,16)]] for exchanging data between the associated buffer [[(11,12)]] and said data transfer facility [[(BUS)]], said master block [[(15,16)]] being adapted to be coupled in a data exchange relationship to a buffer in a homologous direct memory access module [[(IDMA)]] in an arrangement wherein said master block [[(15,16)]] and said buffer coupled thereto are configured for: [[-]]

issuing at least one request of a requesting buffer for a buffer coupled therewith to indicate at least one transfer condition selected out of the group consisting of [[:]]

data existing to be transferred and enough space existing for receiving said data when transferred; [[-]]

issuing at least one corresponding acknowledgement towards said requesting buffer confirming that the said at least one transfer condition is met; and [[-]]

transferring data between said requesting buffer and said coupled buffer, whereby said data transfer facility [[(BUS)]] is left free between said at least one request and said at least one acknowledgement.

10. (canceled)